**EC772 DESIGN PROJECT –Spring 2013**

**Project Proposal Form**

**The following students:**

|  |  |  |
| --- | --- | --- |
| **Member Name** | **Username** | **Signature** |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

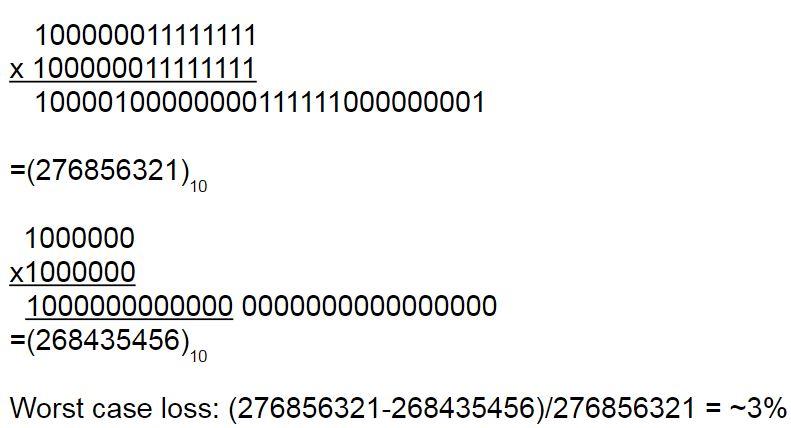
**Request approval of a Design Project entitled:**

|  |
| --- |
| Multicycle CPU with Approximate ALU |

**Write the description of the proposed project:**

**(Include any research sources)**

We plan to build a multicycle CPU with a 32-bit instruction set incorporating an approximate ALU. The CPU accepts both I-type and R-type instructions and can perform operations such as addition, subtraction, multiplication, and logical operations. Among the operations specified, multiplication consumes the most power for computation and time. For our project, we will focus on significantly improving the multiplication operation.

We have come up with a way to approximate the multiplication computation resulting in low computational loss using less power. Our implementation includes eliminating bits in the multiplicands, executing the multiplication, then concatenating zeros matching the number of bits originally eliminated. The amount of bits eliminated can be distinguished by the user in order to allow for a user defined resolution in the computation. For example, if we have a 16 bit signed integer, if we ignore the last 8 bits, perform the computation, and then concatenate 16 zeros after the result, the worst case percentage error is ~3%.

We eventually want to compare our power and performance to other approximation methods already performed.

**1. List the following:**

**A) Objectives**

1) Verilog code for multicycle CPU

2) Verilog code for multicycle CPU with approximation

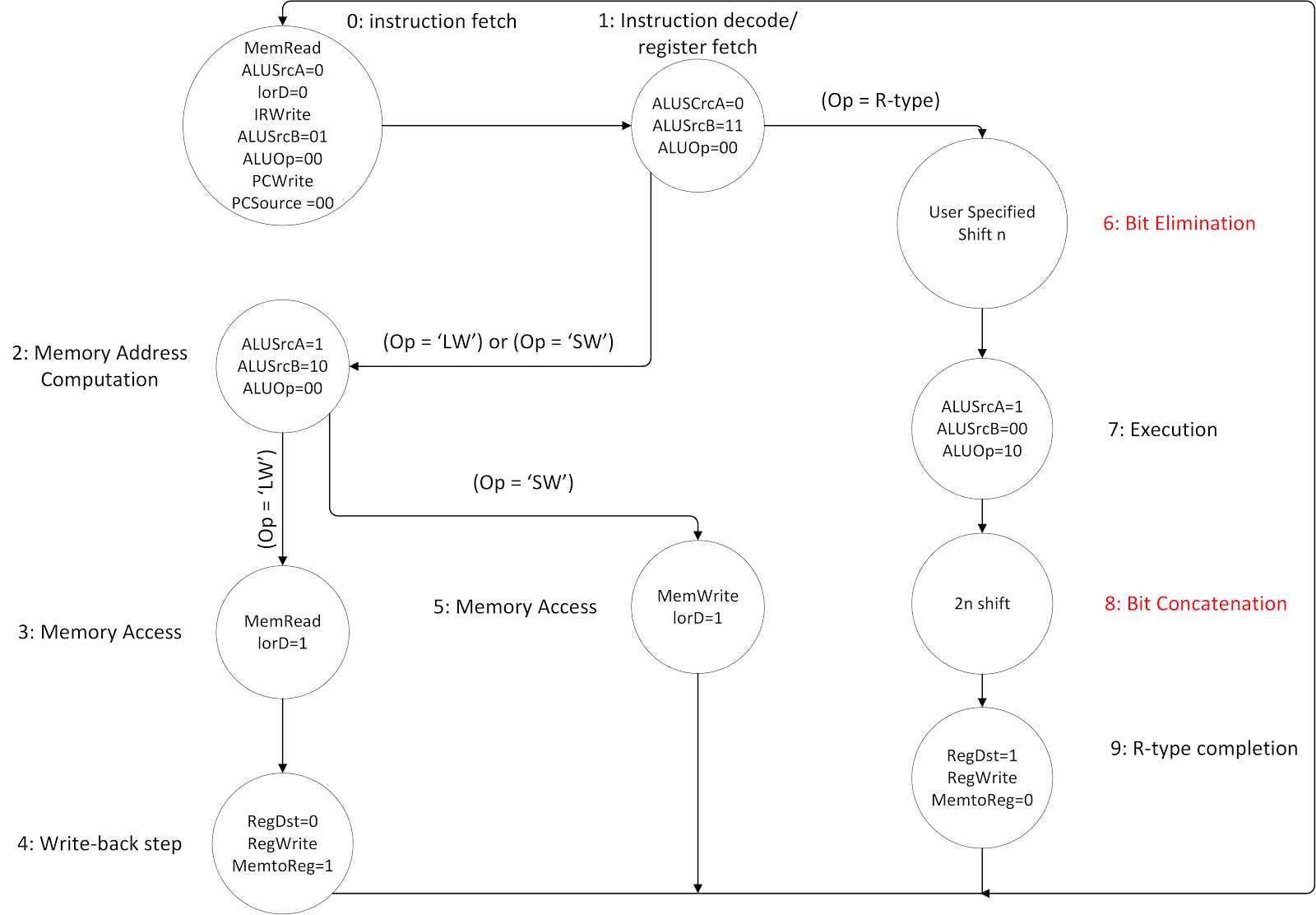
3) Power comparison

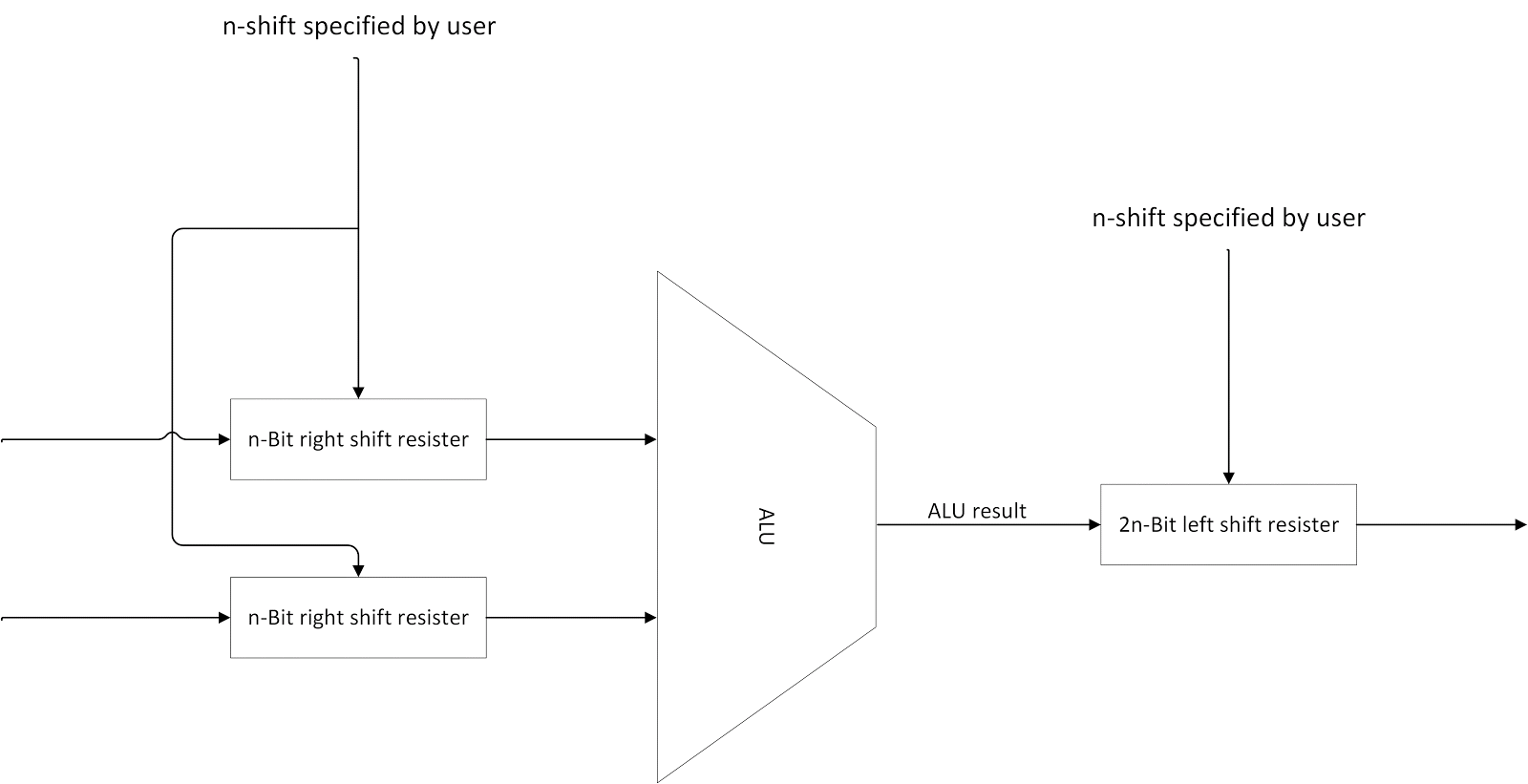
4) Scan path

5) Tool flow to obtain .edif

6) Find most optimum adders for our design

**B) Design Elements (Block Diagrams, etc..)**





**C) Measures of Success**

Successfully synthesizing and completing the design flow of the Cadence tool kit, which would demonstrate our understanding and experience with the tools.

**2. Project Difficulty Rating**

**(Please circle based on group’s overall size and ability)**

**1 2 3 4 5 6 7 8 9 10**

**Very Easy Very Difficult**

**3. If everything goes according to plan, what will be your group’s deliverables in May 2016?**

Complete the design tool flow to perform floorplan and placement. Generate the EDIF file.

A detailed report comparing the power and performance when the CPU is in normal mode and with the different approximation levels.

The CPU ALU with floating point multiplication and its benefits.